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CP319: Digital System Design

Course Syllabus

CP319: Digital Logic Design
Physics & Computer Science, Faculty of Science, Waterloo Campus
Fall 2018

I acknowledge that in Kitchener, Waterloo, Cambridge and Brantford we are on the traditional territory of the Neutral, Anishnawbe, and Haudenosaunee peoples.

Instructor Information

Dr. Ahmed Farouk |Office: N2091A
Contact Information (5195900213 / afarouk@wlu.ca)
Weekly Office Hours (Tuesday 15:00- 15:50, Thursday 17:30-18:30) or By Appointment

Course Information

Study the principles of Logic families and interfacing considerations for logic devices, Verilog HDL; implementation techniques for combinational and sequential logic; introduction to finite state machines and design methodologies for synchronous and asynchronous sequential circuits; hazards, cycles and races; operation and interfacing of memory devices.

Date Range: Sep 06, 2018 - Dec 05, 2018.
Course Location: Dr. Alvin Woods Building 3-106
Meeting Time and Days: 4:00 pm - 5:20 pm TR
3 lecture hours
Credit: 0.50
Cross-Listed: as PC319
Prerequisite: CP104, CP220/PC220 (or CP120/PC120)
Co-requisite: CP300/PC300 recommended

Course Overview and Approach

The course will cover an overview of digital design; two level minimization and implementation; combinational logic implementation technologies; delays, timing and hazards in digital logic; multilevel logic synthesis; arithmetic logic circuits such as adders, Decoders; memory elements and clocking; registers, counters, shifters; flip flops; random access memory and read only memory; sequential logic

design; finite state machine optimization and state assignment; introduction to Verilog HDL; Verilog HDL structural modeling; Verilog HDL behavioral modeling; case studies in Verilog HDL.

By the end of the course the student will be able to design, simulate, build, and debug complex combinational and sequential digital circuits based on an abstract functional specification. The student will also understand the basic internal workings of the central processing unit of a computer and its interface with memory and input/output subsystems. The course gives students sufficient understand and feel comfortable with some fundamental computer architecture terms as the instruction set, microprograms and microinstructions.

Course Goals and Learning Outcomes

By the end of this course students should be able to:

- Design digital systems, from specification and simulation to construction and debugging.
- Have a basic understanding of the building blocks and implementation technologies available to digital designers.
- Manually analysis, design, optimizes, and implements combinational and sequential circuits.
- Understand how to use schematic capture software to design digital circuits.
- Understand that sequential behavior can be specified in different ways and have a reasonably good understanding of how to start from a few different types of specifications and end up with working logic.
- Understand how to design, optimize, and implement finite state machines.
- Understand the differences between synchronous and asynchronous finite state machines and know the advantages of each.
- Be capable of doing Verilog HDL designs and understand the functionality of the design.

Course Tools and Learning Materials

Reference Texts

- Brown, S. D. (2007). Fundamentals of digital logic with Verilog design. Tata McGraw-Hill Education.

- Mano, M. M., & Kime, C. R. (2008). Logic and computer design fundamentals. Upper Saddle River, NJ: Pearson Prentice Hall.

- Hachtel, G. D., & Somenzi, F. (2006). Logic synthesis and verification algorithms. Springer Science & Business Media

Modelsim and Verilog HDL:

- Download ModelSim PE Student Edition
  https://www.mentor.com/company/higher_ed/modelsim-student-edition
  Follow the instructions to receive a free license to install the software.

- Introduction to Verilog
  http://www.doe.carleton.ca/~jknight/97.478/PetervrlK.pdf

- Verilog Tutorials and Examples
  https://www.nandland.com/verilog/tutorials/index.html

- Verilog TUTORIAL for beginners
  http://referencedesigner.com/tutorials/verilog/verilog_01.php

- Verilog Tutorial
  https://ece.umd.edu/class/enee359a.S2007/verilog_tutorial.pdf

- A Free self-study course for learning the Verilog Hardware Description Language
  http://vol.verilog.com/

*** More resources will be added online.**

Student Evaluation

Assessment	**Weighting**
Assignments	25%
Quizzes	15%
Homework	15%
Midterm Exam	15%
Final Exam	30%
Total	**100%**

Assignments and Homework

- No late assignment / Homework (will get a grade of 0).
- Assignments / Homework must be submitted online on MyLS. If not mentioned other
- Assignments are worth 25% of your final grade. Each of the first 3 assignments is worth 5%. Assignment 4 is worth more, at 10% of the final grade. Homework is worth 15% of your final grade.
- Due Friday at 11:30 PM
- Due dates for the assignments and homework are listed below.
- All assignment work is done individually on your own, there is no group work allowed, except for assignment 4. It is considered Academic Misconduct to provide your work to another student for any reason.

Extensions

Students who cannot meet an assignment deadline are required to communicate with the course instructor in writing (normally by email). This consultation must occur before the assignment is due and during the normal workweek. If the instructor is not consulted prior to the due date, the assignment will not normally be accepted.

Normally, the only acceptable reasons for an extension for assignments (with no penalty) are serious illness or extreme compassionate circumstances (documentation may be required).

Missed Assignments

An assignment not handed in receives a mark of 0, unless there is a documented reason. If a documented reason is supplied, the weight of the missing assignment is shifted to the final exam. A copy of the documented reason must be given to and approved by the instructor.

Midterms

Tuesday, October 23, 2018, in class.

Missed Midterm

A missed midterm exam will receive a mark of 0, unless there is a valid documented reason. If a documented reason is provided midterm for missing the midterm, its weight is applied to the final exam.

Final Exam

To be announced by the registrar office.

Assignments and Homework due Date Time Table

Activity	Due Date
Assignment 1	Friday, 21 September , 11:30 PM
Assignment 2	Friday, 12 October , 11:30 PM
Assignment 3	Friday, 9 November , 11:30 PM
Assignment 4	Friday, 30 November , 11:30 PM
Homework 1	Friday, 21 September , 11:30 PM
Homework 2	Friday, 2 November , 11:30 PM
Homework 3	Friday, 5 October , 11:30 PM
Homework 4	Friday, 16 November , 11:30 PM

Weekly Schedule(s) (lecture, lab, seminars, tutorials, etc.)

Note: this schedule is subject to change.

Week	Start	Theory	Lab Assignment	Homework	Others
1	September 02	Previous knowledge: A review			
2	September 09	Combinational Circuit I		Homework 1	
3	September 16	Combinational Circuit II	Assignment 1		
4	September 23	Flip-Flops, Registers, and Counters			Quiz 1

Week	Start	Theory	Lab Assignment	Homework	Others
5	September 30	Sequential Circuits I		Homework 2	
6	October 07	Sequential Circuits II	Assignment 2		
7	October 14	Reading Week			
8	October 21	Sequential Circuits III			Midterm Exam, Tuesday , October 23
9	October 28	Finite State Machine I		Homework 3	
10	November 04	Finite State Machine II	Assignment 3		Quiz 2
11	November 11	Optimized Implementation of Logic Functions		Homework 4	
12	November 18	Memory and Programmable Logic I			Quiz 3
13	November 25	Memory and Programmable Logic II	Assignment 4		

University and Course Policies (proposed and required text)

1. **Academic Calendars:** Students are encouraged to review the Academic Calendar for information regarding all important dates, deadlines, and services available on campus.

2. **Special Needs:** Students with disabilities or special needs are advised to contact Laurier's Accessible Learning Centre for information regarding its services and resources.

3. **Plagiarism:** The University has approved the following wording for inclusion on all course syllabi about the use of the institutionally supported plagiarism software tool. "Wilfrid Laurier University uses software that can check for plagiarism. If requested to do so by the instructor, students are required to submit their written work in electronic form and have it checked for plagiarism." (Approved by Senate May 14, 2002).

4. **Academic Integrity:** Laurier is committed to a culture of integrity within and beyond the classroom. This culture values trustworthiness (i.e., honesty, integrity, and reliability), fairness, caring, respect, responsibility and citizenship. Together, we have a shared responsibility to uphold this culture in our academic and nonacademic behaviour. The University has a defined policy with respect to academic misconduct. As a Laurier student you are responsible for familiarizing yourself with this policy and the accompanying penalty guidelines, some of which may appear on your transcript if there is a finding of misconduct. The relevant policy can be found at Laurier's academic integrity website along with resources to educate and support you in upholding a culture of integrity. Ignorance is not a defense.

5. **Classroom Use of Electronic Devices:** State your classroom practice and any consequences for student failure to comply – see Policy 9.3 (Approved by Senate March 8, 2012).

6. **Late Assignment Policy:** Specify any penalties that will be assessed when deadlines for the completion of course components are not met (Approved by Senate May 23, 2012). Refer to the Handbook on Undergraduate Course Management for more information.

7. **Final Examinations:** Students are strongly urged not to make any commitments (i.e., vacation) during the examination period. Students are required to be available for examinations during the examination periods of all terms in which they register. Refer to the Handbook on Undergraduate Course Management for more information.

8. **Foot Patrol, the Wellness Centre, and the Student Food Bank:** The University approved the inclusion of information about select wellness and safety services and supports on campus in the course information provided to students. (Approved by Senate November 28, 2011.) Specific language (by campus) is provided below.

Other course policies:

- Students will have two weeks after a mark is posted to dispute the mark. After two weeks, no changes will be made. It is the responsibility of the student to ensure all grades are posted in MyLearningSpace.
- Grades will not be changed after the final exam has ended regardless of circumstances. If you are missing your marks email your Instructional Assistant immediately.
- If you are unable to write the midterms please contact your Course Instructor.
- Students must complete at least 2 / 4 assignments for term work. If you are unable to complete more than 2 assignments please contact your Course Instructor. No assignments will be dropped. If you fail to complete an assignment, lab exam, or quiz, your mark will be 0 for missed assessments, or partial marks for work not completed.

Guidelines for Technology use During Class and During Course Assessment

- Adhering to the University's policy on the use of electronic devices (see above) it is important for you to realize that the use of electronic devices such as cellphones, laptops, and tablets for non-academic use during lectures, labs, and assessments is prohibited.
- Answering messages, using social networking sites, or gaming are distracting practices that reduce the ability for you to learn the material that is provided. You are a distraction to others in the room as well as the instructor, so electronic devices will only be used for academic purposes.
- I'll request that your cellphone is turned off and put away during lectures, labs, and midterms so you do not distract others, and so that your potential for learning is increased. If you have personal reasons that require the use of a cellphone for emergency contact reasons, please contact me to discuss them so we can make appropriate arrangements.

Multi-campus Resource:

- Good2Talk is a postsecondary school helpline that provides free, professional and confidential counselling support for students in Ontario. Call 1-866-925-5454 or through 2-1-1. Available 24-7.

Kitchener/Waterloo Resources:

- Waterloo Student Food Bank: All students are eligible to use this service to ensure they're eating healthy when overwhelmed, stressed or financially strained. Anonymously request a package online 24-7. All dietary restrictions accommodated.

- Waterloo Foot Patrol: 519.886.FOOT (3668). A volunteer operated safe-walk program, available Fall and Winter daily from 6:30 pm to 3 am. Teams of two are assigned to escort students to and from campus by foot or by van.

- Waterloo Student Wellness Centre: 519-884-0710, x3146. The Centre supports the physical, emotional, and mental health needs of students. Located on the 2nd floor of the Student Services Building, booked and same-day appointments are available Mondays and Wednesdays from 8:30 am to 7:30 pm, and Tuesdays, Thursdays and Fridays from 8:30 am to 4:15 pm. Contact the Centre at x3146, wellness@wlu.ca or @LaurierWellness. After hours crisis support available 24/7. Call 1-844-437-3247 (HERE247).